CLAIMS

1. A memory array comprising:

first and second isolation regions situated in a substrate, said first and second isolation regions being separated by a separation distance;

a trench situated between said first and second isolation regions, said trench defining trench sidewalls and a trench bottom in said substrate;

a tunnel oxide layer situated between said first and second isolation regions, said tunnel oxide layer being situated on said trench sidewalls and said trench bottom;

a channel region situated underneath said tunnel oxide layer, said channel region extending along said trench sidewalls and said trench bottom, said channel region having an effective channel width, wherein said effective channel width corresponds to a height of said trench sidewalls;

wherein said effective channel width is greater than said separation distance between said first and said second isolation regions.

2. The memory array of claim 1 wherein an increase in said height of said trench sidewalls causes an increase in said effective channel width.

3. The memory array of claim 2 wherein said increase in said effective channel width causes an increase in a drive current in said memory array.

4. The memory array of claim 1 further comprising a floating gate layer

situated over said tunnel oxide layer, said floating gate layer being situated in said trench.

5. The memory array of claim 4 further comprising an ONO stack situated over said floating gate layer.

6. The memory array of claim 5 further comprising a word line situated over said ONO stack.

7. The memory array of claim 1 wherein said memory array is a floating gate flash memory array.

8. A memory array comprising first and second isolation regions situated in a substrate, said first and second isolation regions being separated by a separation distance, a tunnel oxide layer situated between said first and second isolation regions, a channel region situated underneath said tunnel oxide layer, said memory array being characterized by:

a trench situated between said first and second isolation regions, said trench defining trench sidewalls and a trench bottom in said substrate, said tunnel oxide layer being situated on said trench sidewalls and said trench bottom, said channel region extending along said trench sidewalls and said trench bottom, said channel region having an effective channel width, wherein said effective channel width corresponds

to a height of said trench sidewalls, wherein said effective channel width is greater than said separation distance between said first and second isolation regions.

9. The memory array of claim 8 wherein an increase in said height of said trench sidewalls causes an increase in said effective channel width.

10. The memory array of claim 8 wherein said increase in said effective channel width causes an increase in a drive current in said memory array.

11. The memory array of claim 8 further comprising a floating gate layer situated over said tunnel oxide layer, said floating gate layer being situated in said trench.

12. The memory array of claim 11 further comprising an ONO stack situated over said floating gate layer.

13. The memory array of claim 12 further comprising a word line situated over said ONO stack.

14. The memory array of claim 8 wherein said memory array is a floating gate flash memory array.

15. A method for fabricating a memory array, said method comprising steps of:

forming a trench between first and second isolation regions in a substrate, said trench defining trench sidewalls and a trench bottom in said substrate, said first and second isolation regions being separated by a separation distance;

forming a tunnel oxide layer between said first and second isolation regions, said tunnel oxide layer being formed on said trench sidewalls and said trench bottom;

forming a channel region underneath said tunnel oxide layer, said channel region extending along said trench sidewalls and said trench bottom, said channel region having an effective channel width, wherein said effective channel width corresponds to a height of said trench sidewalls;

wherein said effective channel width is greater than said separation distance between said first and second isolation regions.

16. The method of claim 15 wherein an increase in said height of said trench sidewalls causes an increase in said effective channel width.

17. The method of claim 16 wherein said increase in said effective channel width causes an increase in a drive current in said memory array.

18. The method of claim 15 further comprising a step of forming a floating gate layer over said tunnel oxide layer and in said trench.

19. The method of claim 18 further comprising a step of forming an ONO stack over said floating gate layer.

20. The method of claim 19 wherein said memory array is a floating gate flash memory array.